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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,472	08/29/2001	Katsuji Kimura	Q65962	4891

7590 09/24/2002

SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 Pennsylvania Avenue, N.W.
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EXAMINER
NGUYEN, MINH T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/940,472	Applicant(s) KIMURA, KATSUJI	
	Examiner Minh Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *5-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on 7/31/02 has been received and entered in the case. The amendment and argument presented therein overcome the informality objections and indefiniteness rejections, and therefore, are withdrawn. Since claims 5-13 are drawn to a non-elected group without traverse, these claims should be requested to be canceled in the next response. Due to the misinterpretation of Figure 1 as pointed out by the Applicant, this action is NON FINAL even though the same reference is used for prior art rejection in this Office Action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,602,509, issued to Kimura.

As per claim 1, Kimura discloses a voltage subtractor/adder circuit (Fig. 1, note that Fig. 3 is a functional block diagram of Fig. 1) comprising:

a differential pair (transistors M56 and M57) having a first MOS transistor M56 and a second MOS transistor M57, wherein the gate electrodes of the first and second MOS transistors

forming input terminals, i.e., the gate terminals of M56 and M57, for receiving an input differential voltage (V1-V2), the drain electrodes of the first and second MOS transistors forming output terminals for outputting a signal to be subtracted I (column 2, lines 16-17, Fig. 3, the active load 3 is the subtractor circuit since the circuit outputs the differential output current, column 2, lines 61-64, Fig. 1, transistors M58 and M59 is an active load), and source electrodes of M56 and M57 coupled to form an output terminal B for addition output voltage (the voltage at node B); and

the limitation recited on the last three lines is met as described in column 2, line 22.

As per claim 2, the recited level shifter for level shifting the addition output voltage reads on transistor M55 (column 2, lines 52-55).

As per claim 3, Kimura discloses a voltage subtractor/adder circuit (Fig. 1) comprising:

a differential pair (transistors M56 and M57) having a first MOS transistor M56 and a second MOS transistor M57, wherein the gate electrodes of the first and second MOS transistors forming input terminals, i.e., the gate terminals of M56 and M57, for receiving an input differential voltage (V1-V2), the drain electrodes forming output terminals to the subtractor circuit (M58-M59) for outputting a subtraction output signal i, and source electrodes of M56 and M57 coupled to form an output terminal B for addition output voltage (the voltage at node B); and

a constant current source aI which drives the differential pair (M56 and M57).

As per claim 4, the recited level shifter for level shifting the addition output voltage reads on transistor M55 (column 2, lines 52-55).

Response to Arguments

3. Applicant's arguments filed 7/31/02 have been fully considered but they are not persuasive.

Regarding the argument that circuit 3 (Fig. 1, M51-M54) of Kimura is not a subtractor circuit but rather this circuit is a "cross-coupled quad cell".

The examiner agrees, however, this is a typo mistake because as shown in Fig. 3, the subtractor circuit is the circuit 3 which outputs the signal to be subtracted delta(I). As disclosed in column 2, line 10, Kimura clearly discloses that Fig. 3 is a functional block diagram of Fig. 1; in column 2, lines 16-17, Kimura discloses that the current delta(I) is the differential output current which is derived through the active load 3; in column 2, lines 61-64, Kimura discloses that transistors M58 and M59 in Fig. 1 serving as an active load.

Other arguments are moot when transistors M58 and M59 are seen as the subtractor.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Examiner
Art Unit 2816

MN
September 19, 2002